CLAIMS

1. (Original) An integrated circuit apparatus for facilitating the interconnection of one or more circuitry manufacture, comprising:

a carrier substrate defining a top surface and a bottom surface, the carrier substrate configured to receive one or more circuitry manufacture on the top surface and the bottom surface;

one or more carrier substrate vias penetrating the carrier substrate so that the carrier substrate vias define vias from the top surface to the bottom surface of the carrier substrate and further define interior via surfaces, the one or more carrier substrate vias configured to receive one or more circuitry manufacture on the interior via surfaces; and

one or more carrier substrate cavities, the one or more carrier substrate cavities formed on the top and/or bottom surfaces of the carrier substrate, the one or more carrier substrate cavities defining interior cavity surfaces and configured to receive one or more circuitry manufacture on the interior cavity surfaces.

2. (Original) The integrated circuit apparatus of claim 1, further comprising an electrically conductive material deposited on the interior via surface of one or more carrier substrate vias to form an electrical conductive path from the top surface of the carrier substrate to the bottom surface of the carrier substrate.

3. (Original) The integrated circuit apparatus of claim 2, further comprising a first thin film interconnect formed on the top surface of the carrier substrate and a second thin film interconnect formed on the bottom surface of the carrier substrate, the first and second thin film interconnect defining a first pad layer and a second pad layer and further comprising one or

more conductive paths from the first and second pad layers to the electrically conductive material deposited on the interior via surfaces.

4. (Original) The integrated circuit apparatus of claim 2, further comprising first circuitry mounted to the carrier substrate by one or more circuitry manufacture and atop a carrier substrate cavity.

5. (Original) The integrated circuit apparatus of claim 4, wherein the first circuitry comprises a Micro Electro Mechanical System (MEMS) device.

6. (Original) The integrated circuit apparatus of claim 5, further comprising second circuitry mounted to the carrier substrate by one or more circuitry manufacture and proximate to one or more substrate vias.

7. (Original) The integrated circuit apparatus of claim 6, wherein the second circuitry comprises an integrated circuit operable to communicate data to and from the MEMS device, and wherein the integrated circuit is in electrical communication with the MEMS device through one or more conductive paths deposited on the interior surfaces of the substrate vias.

8. (Original) The integrated circuit apparatus of claim 2, further comprising first circuitry mounted to the carrier substrate by one or more circuitry manufacture and within a carrier substrate cavity.

9. (Original) The integrated circuit apparatus of claim 8, further comprising second circuitry mounted to the carrier substrate by one or more circuitry manufacture and atop the carrier substrate cavity.

10. (Original) The integrated circuit apparatus of claim 9, wherein the first circuitry comprises a passive circuit device and the second circuitry comprises a Micro Electro

Mechanical System (MEMS) device, and wherein the MEMS device is in electrical communication with the passive circuit device.

11. (Original) The integrated circuit apparatus of claim 3, wherein the first pad layer defines a first metallurgy and the second pad layer defines a second metallurgy.

12. The integrated circuit apparatus of claim 11, wherein the first metallurgy is a wire bonding pad metallurgy and the second metallurgy is a Ball Grid Array (BGA) metallurgy.

13. (Original) The integrated circuit apparatus of claim 1, wherein the one or more carrier substrate vias are in proximate disposition to the carrier substrate cavities.

14. (Withdrawn) The integrated circuit apparatus of claim 1, further comprising one or more carrier substrate cavity vias penetrating the carrier substrate so that the carrier substrate cavity vias define vias from a bottom surface of one or more carrier substrate cavities to the bottom surface of the carrier substrate and further define interior via surfaces, the one or more carrier substrate cavity vias configured to receive one or more circuitry manufacture on the interior via surfaces.

15. (Original) The integrated circuit apparatus of claim 1, wherein the carrier substrate is silicon.

16. (Original) The integrated circuit apparatus of claim 1, wherein the one or more circuitry manufacture comprises a conductive material.

17. (Withdrawn) A method for facilitating the interconnection of one or more circuitry manufacture, comprising:

providing a carrier substrate defining a top surface and a bottom surface,

creating one or more carrier substrate vias penetrating the carrier substrate so that the carrier substrate vias define vias from the top surface to the bottom surface of the carrier substrate and further define interior via surfaces; and

creating one or more carrier substrate cavities on the top and/or bottom surfaces of the carrier substrate so that the one or more carrier substrate cavities define interior cavity surfaces;

wherein the top and bottom surfaces of the carrier substrate, the interior via surfaces, and the interior cavity surfaces are configured to receive one or more circuitry manufacture.

18. (Withdrawn) The method of claim 17, further comprising depositing an electrically conductive material on the interior via surface of one or more carrier substrate vias to form an electrical conductive path from the top surface of the carrier substrate to the bottom surface of the carrier substrate.

19. (Withdrawn) The method of claim 18, further comprising:

forming a first thin film interconnect on the top surface of the carrier substrate;

forming a second thin film interconnect on the bottom surface of the carrier substrate;

forming a first pad layer on the first thin film interconnect;

forming a second pad layer on the second thin film interconnect; and

forming one or more conductive paths from the first and second pad layers to the electrically conductive material deposited on the interior via surfaces.

20. (Withdrawn) The method of claim 19, wherein forming a first pad layer on the first thin film interconnect comprises forming a first pad layer of a first metallurgy and forming a second pad layer on the second thin film interconnect comprises forming a second pad layer of a second metallurgy.

21. (Withdrawn) The method of claim 18, further comprising:

attaching by one or more circuitry manufacture a first circuitry to the carrier substrate atop a carrier substrate cavity and proximate to one or more carrier substrate vias;

attaching by one or more circuitry manufacture a second circuitry to the carrier substrate and proximate to one or more carrier substrate vias; and

electrically connecting the first circuitry to the second circuitry through the electrical conductive paths on the one or more interior via surfaces.

22. (Withdrawn) The method of claim 21, wherein the first circuitry comprises a Micro Electro Mechanical System (MEMS) device and the second circuitry comprises an integrated circuit operable to communicate data to and from the MEMS device.

23. (Withdrawn) The method of claim 17, further comprising creating one or more carrier substrate cavity vias penetrating the carrier substrate so that the carrier substrate cavity vias define vias from a bottom surface of a carrier substrate cavity to the bottom surface of the carrier substrate and further define interior via surfaces configured to receive one or more circuitry manufacture.

24. (Withdrawn) The method of claim 17, wherein the one or more circuitry manufacture comprises a conductive material.

25. (Original) An integrated circuit apparatus for facilitating the interconnection of one or more circuitry manufacture, comprising:

means for defining a top carrier substrate surface and a bottom carrier substrate surface and for receiving one or more circuitry manufacture on the top carrier substrate surface and the bottom carrier substrate surface;

means for defining vias from the top carrier substrate surface to the bottom carrier substrate surface and for defining interior via surfaces for receiving one or more circuitry manufacture; and

means for defining cavity surfaces on the top and/or bottom carrier substrate surfaces and for receiving one or more circuitry manufacture on the interior cavity surfaces.

26. (Original) The integrated circuit apparatus of claim 25, further comprising means for creating an electrically conductive connection through the means for defining vias on the interior via surfaces.

27. (Original) An integrated circuit, comprising:

a carrier substrate defining a top surface and a bottom surface, the carrier substrate configured to receive one or more circuitry manufacture on the top surface and the bottom surface;

one or more carrier substrate vias penetrating the carrier substrate so that the carrier substrate vias define vias from the top surface to the bottom surface of the carrier substrate and further define interior via surfaces, the one or more carrier substrate vias configured to receive one or more circuitry manufacture on the interior via surfaces;

one or more carrier substrate cavities, the one or more carrier substrate cavities formed on the top and/or bottom surfaces of the carrier substrate, the one or more carrier substrate cavities defining interior cavity surfaces and configured to receive one or more circuitry manufacture on the interior cavity surfaces;

a first circuit device mounted to the carrier substrate and further mounted relative to a carrier substrate cavity by one or more circuitry manufacture; and

a second circuit device mounted to the carrier substrate by one or more circuitry manufacture and in electrical communication with the first circuit device.

28. (Original) The integrated circuit of claim 27, wherein the first circuit device comprises a Micro Electro Mechanical System (MEMS) device.

29. (Original) The integrated circuit of claim 28, wherein the MEMS device is mounted relative to the carrier substrate cavity by one or more circuitry manufacture by mounting the MEMS device in the carrier substrate cavity.

30. (Original) The integrated circuit of claim 28, wherein the MEMS device is mounted relative to the carrier substrate cavity by one or more circuitry manufacture by mounting the MEMS device atop the carrier substrate cavity.

31. (Original) The integrated circuit of claim 28, wherein the second circuit device is in electrical communication with the MEMS device through one or more carrier substrate vias and circuitry manufacture deposited in the carrier substrate vias.

32. (Original) The integrated circuit of claim 28, wherein the one or more circuitry manufacture mounting the first and second circuit devices to the carrier substrate comprises a thin film interconnect.